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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/631,830	08/03/2000	Yusuke Kohyama	1701.00021	9692

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BANNER & WITCOFF
1001 G STREET N W
SUITE 1100
WASHINGTON, DC 20001

EXAMINER
MALSAWMA, LALRINFAMKIM HMAR

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/631,830	KOHYAMA ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-29 and 34-39* is/are allowed.

6)☒ Claim(s) *20-22,25,26 and 30-32* is/are rejected.

7)☒ Claim(s) *23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/720,032* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 25 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claims 25 and 26:

These claims contain limitations for the protective film being composed of a second conductive film, wherein the process step(s) for forming said protective film renders the instant claims indefinite because of the following reason:

In Claim 20, the protective film is formed on the (first) conductive film, then the protective film and the (first) conductive film are locally etched to form first and second wirings, followed by forming the second insulating film between said first and second wirings and using said protective film as a mask to form the contact hole; in the instant claims, the process for forming the protective film includes forming a third conductive film on a second conductive film, on the second insulating film, and in the contact hole; therefore, it is not clear ***how*** the protective film (comprising the second and third conductive films) and the (first) conductive film ***can be*** locally etched to form the first and second wirings, since the third conductive film (i.e., a portion of the protective film) must be formed at least after an etching step that defines the contact hole, in other words, it is not clear how the protective film (comprising the third

conductive film) can be used as a mask (note Claim 20, lines 13-14) to form the contact hole, if a portion of the protective film (i.e., the third conductive film) must fill up the contact hole?

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 20 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Havemann (5,482,894).

Regarding Claim 20:

Havemann discloses (in Figs. 1A-1C; Figs. 2A-2C; col. 3, line 54 to col. 4, line 6; and col. 5, lines 2-15) a method of manufacturing a semiconductor storage device comprising the steps of:

forming a first insulating film 22 on a semiconductor substrate 20 (Fig. 1A);

forming a conductive film 10 on said first insulating film (Fig. 1A);

forming a protective film (18 or 28) on said conductive film (Fig. 1A-1C and 2A);

etching said protective film and conductive film locally and forming first and second wirings 26 (Fig. 1B);

forming a second insulating film 30 between said first and second wirings (Fig. 1C and Fig. 2A);

etching said second insulating film 30 and first insulating film 22 locally by using said protective film 28 as a mask and forming a contact hole between said first and second wirings 26 (note process step from Fig. 2A to 2B).

forming a third insulating film 42 at least on a side wall of said conductive film (i.e., wirings 26) and on a side wall of said first insulating film 22 (Fig. 2C). Therefore, the instant claim is anticipated by Havemann.

Regarding Claim 21:

Havemann discloses the step of forming the second insulating film 30 comprises:

depositing said second insulating film 30 on a whole surface (Fig. 2A); and

etching said second insulating film up to the upper surface of said protective film 28 such that the film 30 is removed and the surface of the protective film is planarized (Fig. 2B). Therefore, the instant claim is anticipated.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 22, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann (5,482,894) in view of Ireland (5,466,639).

Regarding Claim 22:

Havemann anticipates the method of Claim 20 but **lacks** forming a linear/space photo-resist which intersects perpendicularly to the first and second wirings, followed by etching the second and first insulating films using the photo-resist and protective film as a mask. It is noted Havemann does not specify any particular process for masking and etching said second and first insulating films, but rather, Havemann discloses the etching process is performed by known methods (note col. 5, lines 5-8). Ireland **teaches** a method of masking and etching at least two insulating layers (40, 10) by utilizing a linear/space photo-resist 42 and a protective film 14 (note Figs. 4-5 and col. 2, lines 54-67). It is noted that Ireland is cited primarily to show that it was well known in the art to etch a plurality of insulating films by utilizing a linear/space photo-resist and a protective film, wherein one of ordinary skill in the art would have realized that locating the linear/space photo-resist in a specific manner would depend on design needs (i.e., locating a linear/space photo-resist perpendicularly to the first and second wirings of Havemann such that contact holes can be etched locally). Furthermore, note Ireland discloses the process of utilizing a photo-resist and a protective film allows a single conductive layer to be deposited in contact holes without forming a resist layer within the contact hole (note in col. 1, lines 43-67, Ireland discloses problems associated with prior art methods). It would have been obvious to one of ordinary skill in the art to modify Havemann as taught by Ireland because Havemann discloses

the second and first insulating films can be etch by known methods, and incorporating a process as taught by Ireland would allow the contact hole to be filled with conductive material without introducing resist into said contact hole.

Regarding Claims 31 and 32:

Havemann discloses a method of manufacturing a semiconductor device comprising:

forming first and second conductive films 26 at a predetermined interval on a first insulating film 22 (Fig. 1B);

forming a second insulating film (28, 30, 32, or 34) on said first conductive film (note Fig. 1D);

forming a photoresist pattern 36 on said second insulating film; and

forming a contact hole in said first and second insulating films located between said first and second conductive films, wherein said contact hole is defined by the photoresist pattern and the first and second conductive films (Fig. 1H).

Havemann **lacks** forming a line/space (photoresist) pattern wherein the line/space pattern perpendicularly intersects the first and second conductive films. Ireland **teaches** a method of forming contacts in semiconductor devices, wherein the method utilizes a line/space photoresist pattern 42 and an insulating layer (14 or 40) underneath the line/space pattern to formed contact holes. Ireland discloses the method can prevent filling the contact holes with resist, since the contact holes are formed by utilizing the line/space photoresist pattern and the underlying insulating layer(s) as a mask. It would have been obvious to one of ordinary skill in the art to modify Havemann by utilizing the contact-hole-forming process taught by Ireland because such

a modification would allow contact holes to be formed without photoresist filling the contact holes.

7. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over of Ireland (5,466,639) in view of Havemann (5,482,894)

Ireland discloses a method of manufacturing a semiconductor device comprising:

forming a first insulating layer 10 on a semiconductor substrate 12 (Fig. 1);

forming a second insulating film 40 on said first insulating layer 10 (Fig. 4);

forming a line/space pattern 42 on said second insulating film (Fig. 5); and

forming a contact hole 52 in said first insulating layer 10 and said second insulating film 40 (Fig. 5-6).

Ireland **lacks** forming first and second wirings, wherein said first and second wirings perpendicularly intersect said line/space pattern. However, it is noted that Ireland discloses only the process steps necessary to form contacts by utilizing a plurality of insulating layers instead of utilizing numerous photoresist-mask patterns (note col. 43-51), wherein the contact-forming process can be incorporated into the manufacture of almost any semiconductor device, and one of ordinary skill in the art would have realized that positioning the line/space pattern in a specific relationship to wiring lines, would be a matter of choice depending on design needs. Havemann is cited to show it was very well known in the art to form first and second wirings having features as currently claimed. Havemann **teaches** (in Figs. 1A-1B) a method of manufacturing a semiconductor device comprising the steps of: forming first and second wirings 26 on a first insulating layer 22 at predetermined intervals, said first and second wirings including a

conductive film 16 and a first insulating film 18 on said conductive film. It would have been an obvious matter of design choice for one of ordinary skill in the art to modify Ireland by incorporating a first and second wiring as taught by Havemann and specifying a particular relationship between the line/space pattern and the wirings because Ireland discloses only pertinent steps for forming contacts without utilizing numerous photoresist masks and Havemann teaches forming wiring structures wherein contacts have to be formed by utilizing the wiring structures to define a contact hole. In other words, utilizing the contact-forming process disclose by Ireland along with the wiring structures of Havemann would result in forming a contact hole, wherein the contact hole is defined by the line/space pattern (of Ireland) and the first and second wirings (of Havemann).

Allowable Subject Matter

8. Claims 27-29 and 34-39 are allowable over the references of record.

9. Claims 23 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claims 27-29 and 34-39:

These claims are allowable primarily because the references of record, singly or in combination, cannot anticipate or render obvious the specific combination of process steps for forming a transistor with a capacitor above a bit line.

Regarding Claims 23 and 24:

These claims are allowable primarily because of the inclusion therein, in combination as currently claimed, of the limitation of removing the protective film (or a portion of the protective film) after the third insulating film is formed.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Okamoto et al. (4,977,105), Mele et al. (5,037,777), Smith et al. (5,055,423), Bollinger et al. (5,200,358), Ogawa et al. (5,275,975), Matsuo et al. (5,312,769), Liou et al. (5,371,041), Fukase et al. (5,578,524), Tsukamoto (5,643,833), Brainerd et al. (5,667,918), and Lin et al. (5,841,195) are cited to show the following: processes for forming contacts utilizing protection layers; methods of forming transistors, capacitors, and bit lines; an methods of forming line/space patterns.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 703-306-5986.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3431 for regular communications and 703-305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Lex Malsawma

March 5, 2002

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800